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# MS-7821

## Intel -Shark Bay plamform Z87

ATX

Ver: 12

CPU:

System Chipset:

Marswell LGA1150

Lynx Point

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Killer E2205

SIO:Fintek NTC6799D

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (800/1066/1333MHz) \* 4 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UP1649-8Phase

Expansion Slots:

Other:

PCI Express (X16) Slot \*3

SATA3.0 x6 (PCH)

PCI Express (X1 ) Slot \* 4

REAR USB2.0 \*2

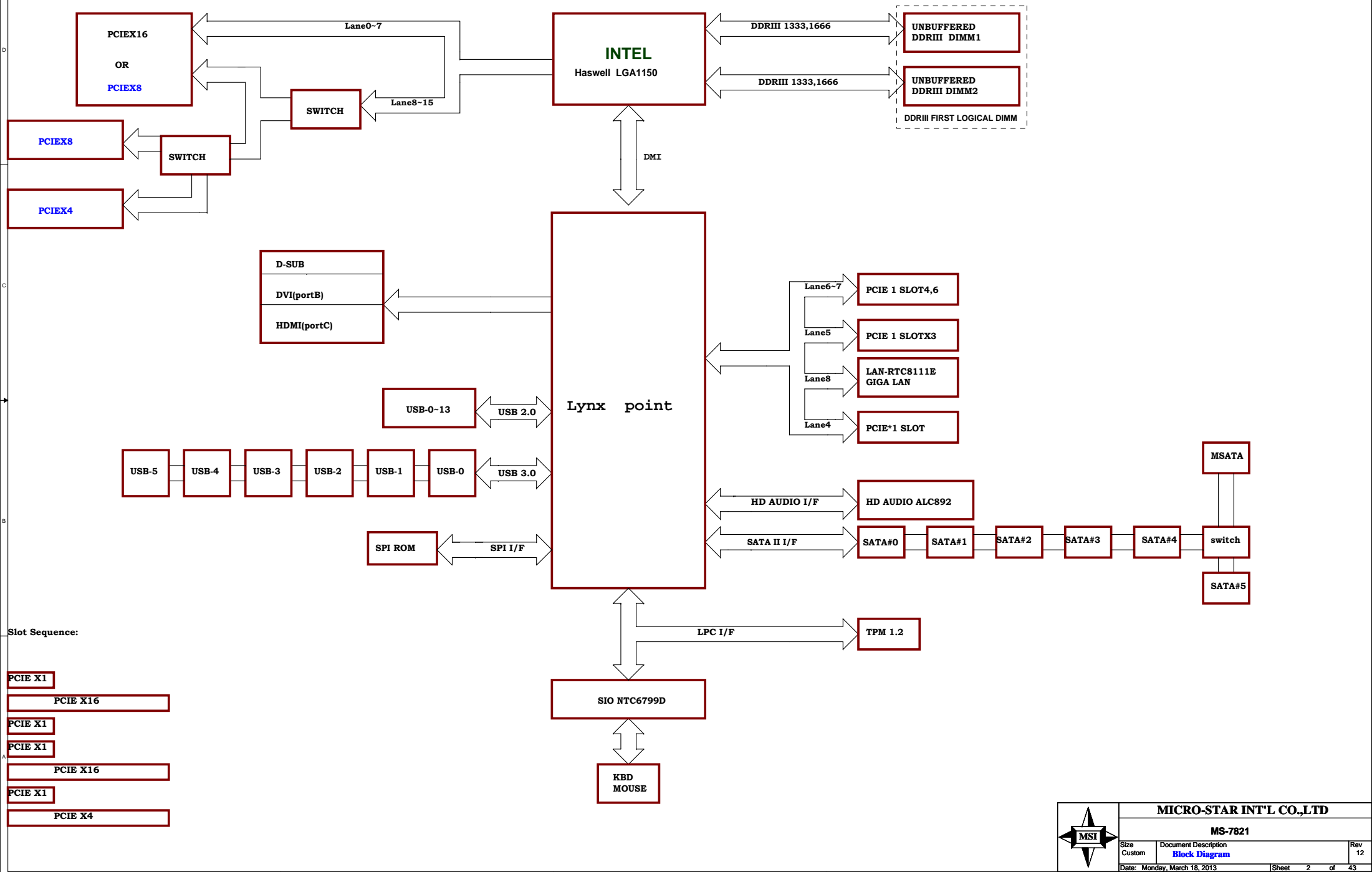
FRONT USB2.0 \*6

REAL USB3.0 \*4

FRONT USB3.0 \*2



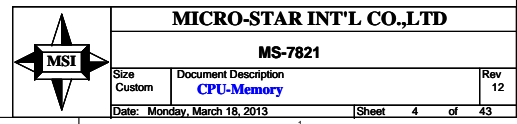
MS-7821 Block Diagram







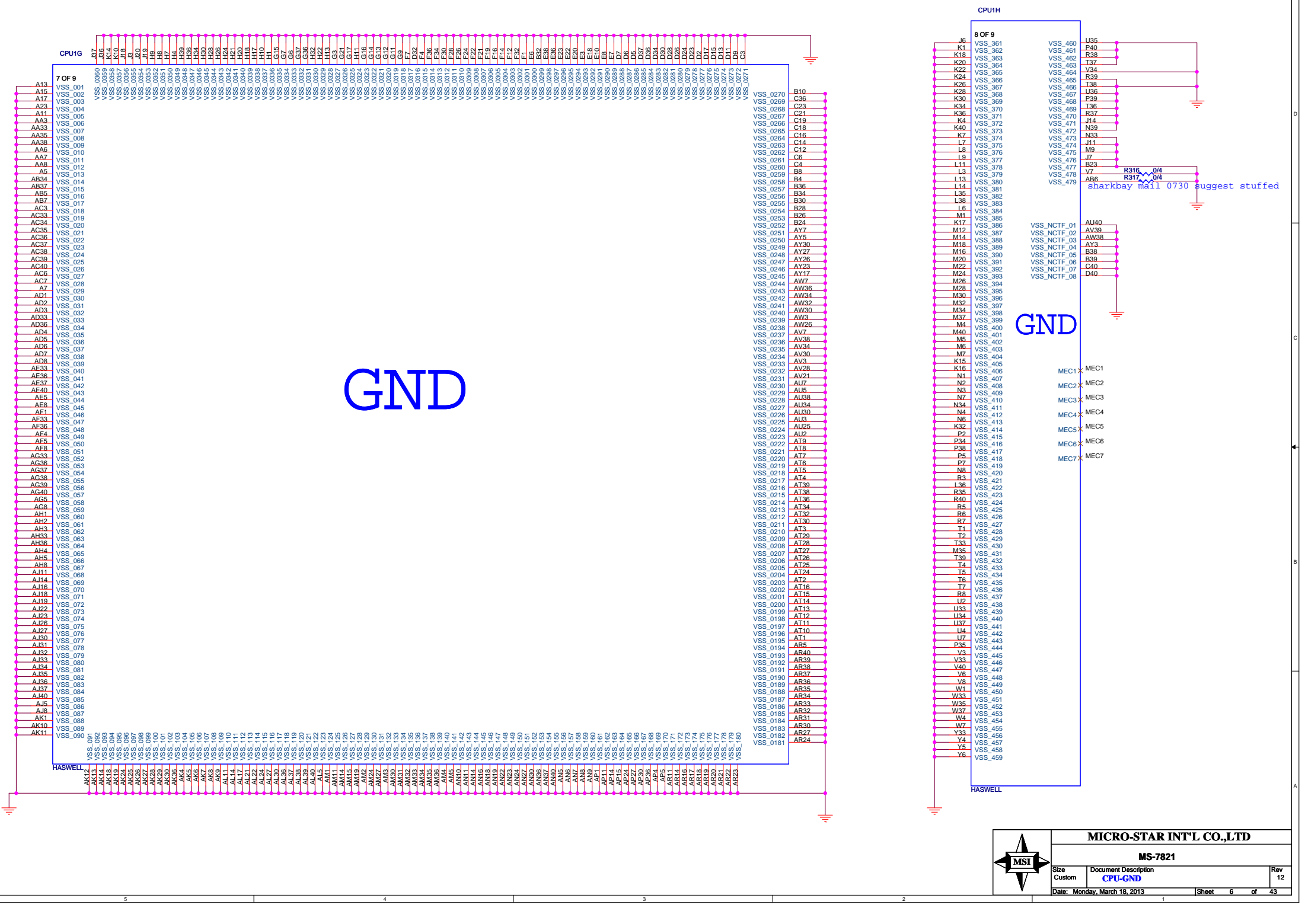




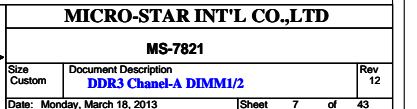








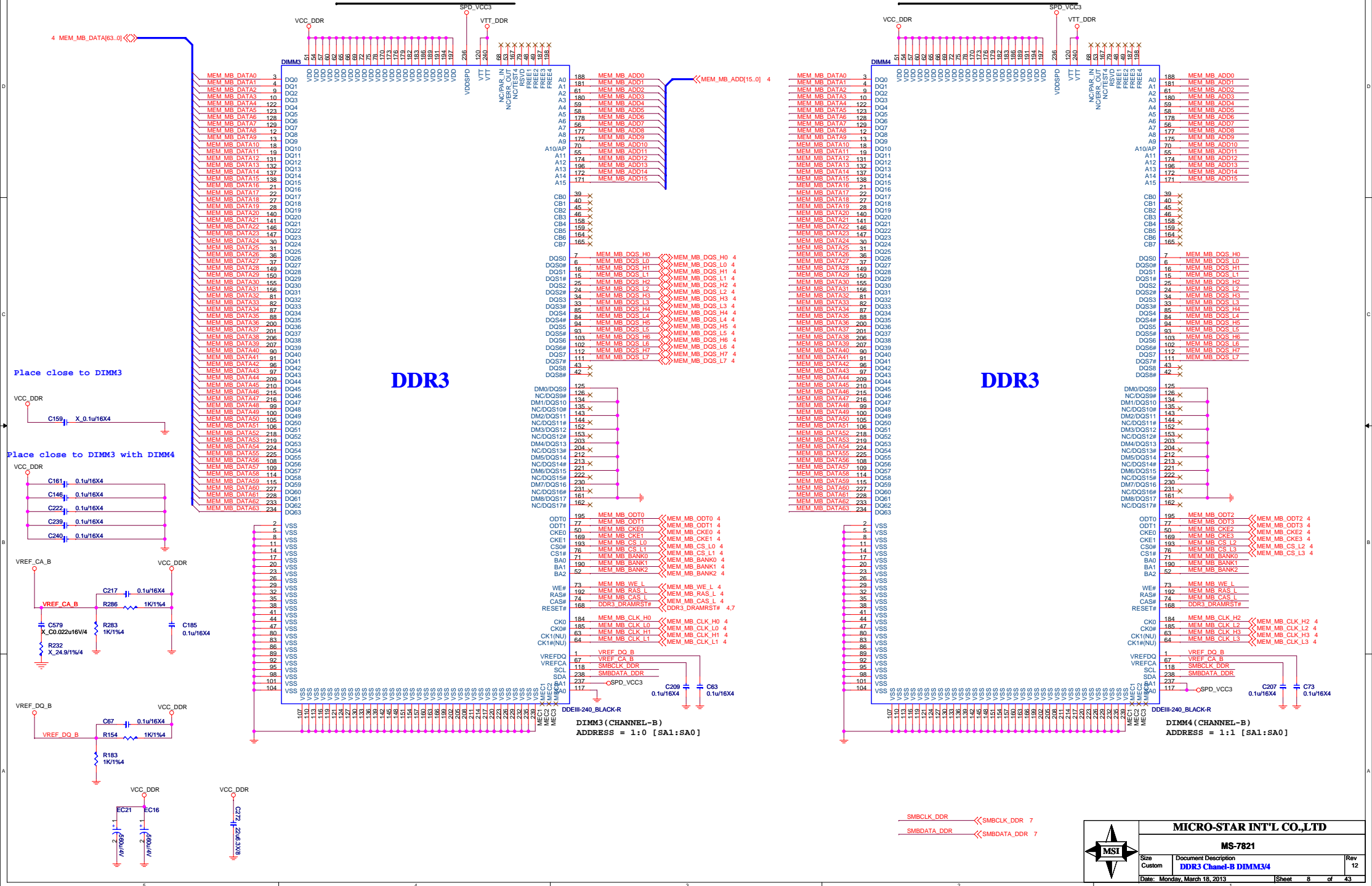




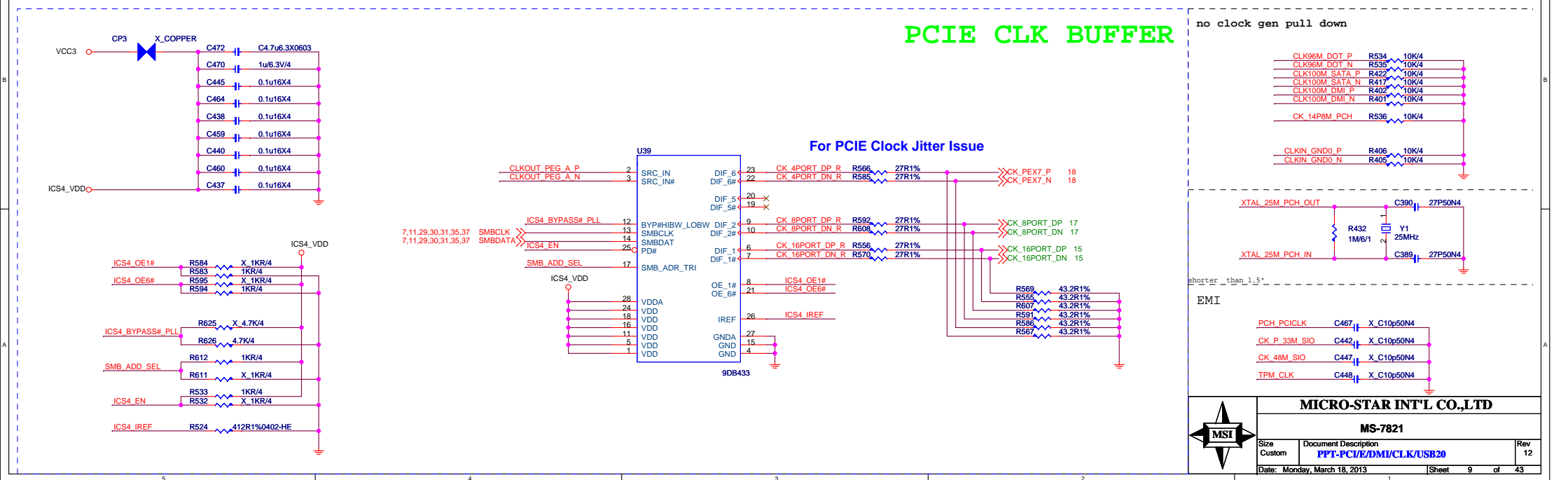
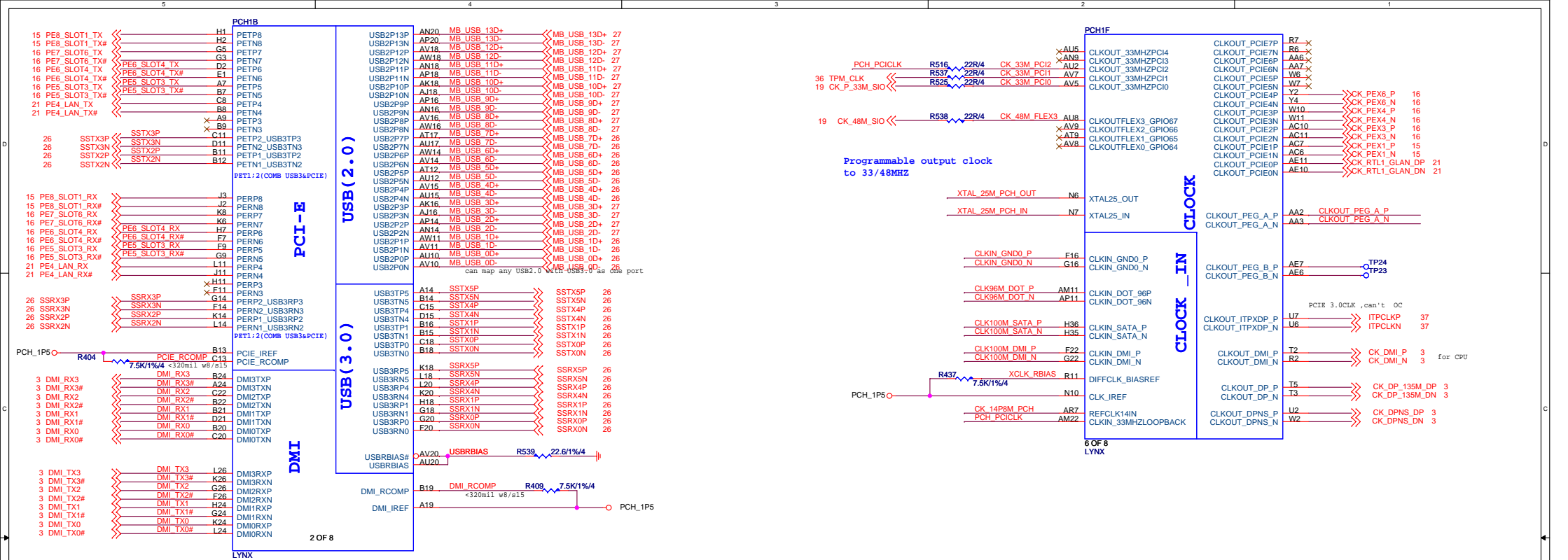


# DDRIII DIMM\_B0

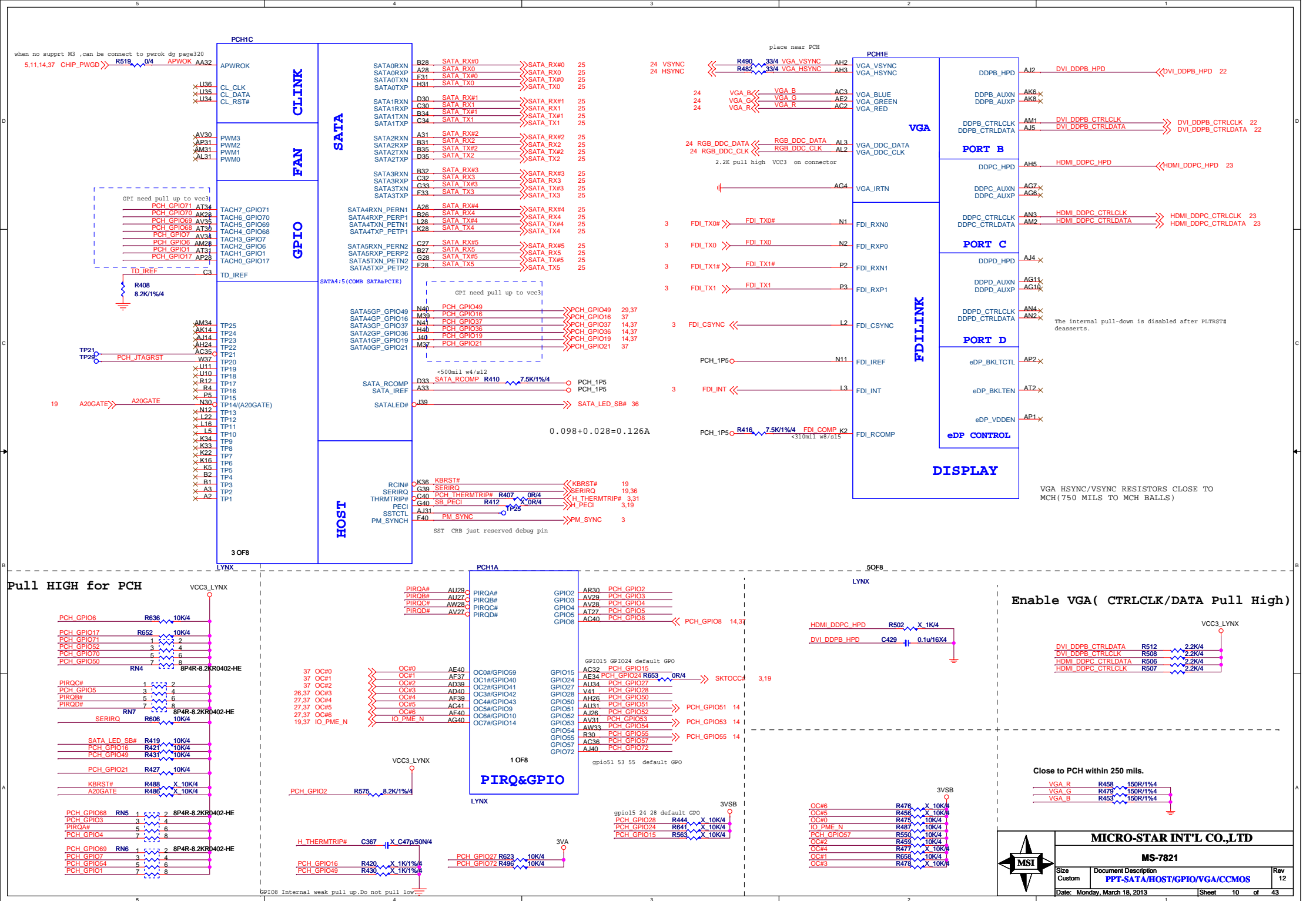
# DDRIII DIMM\_B1



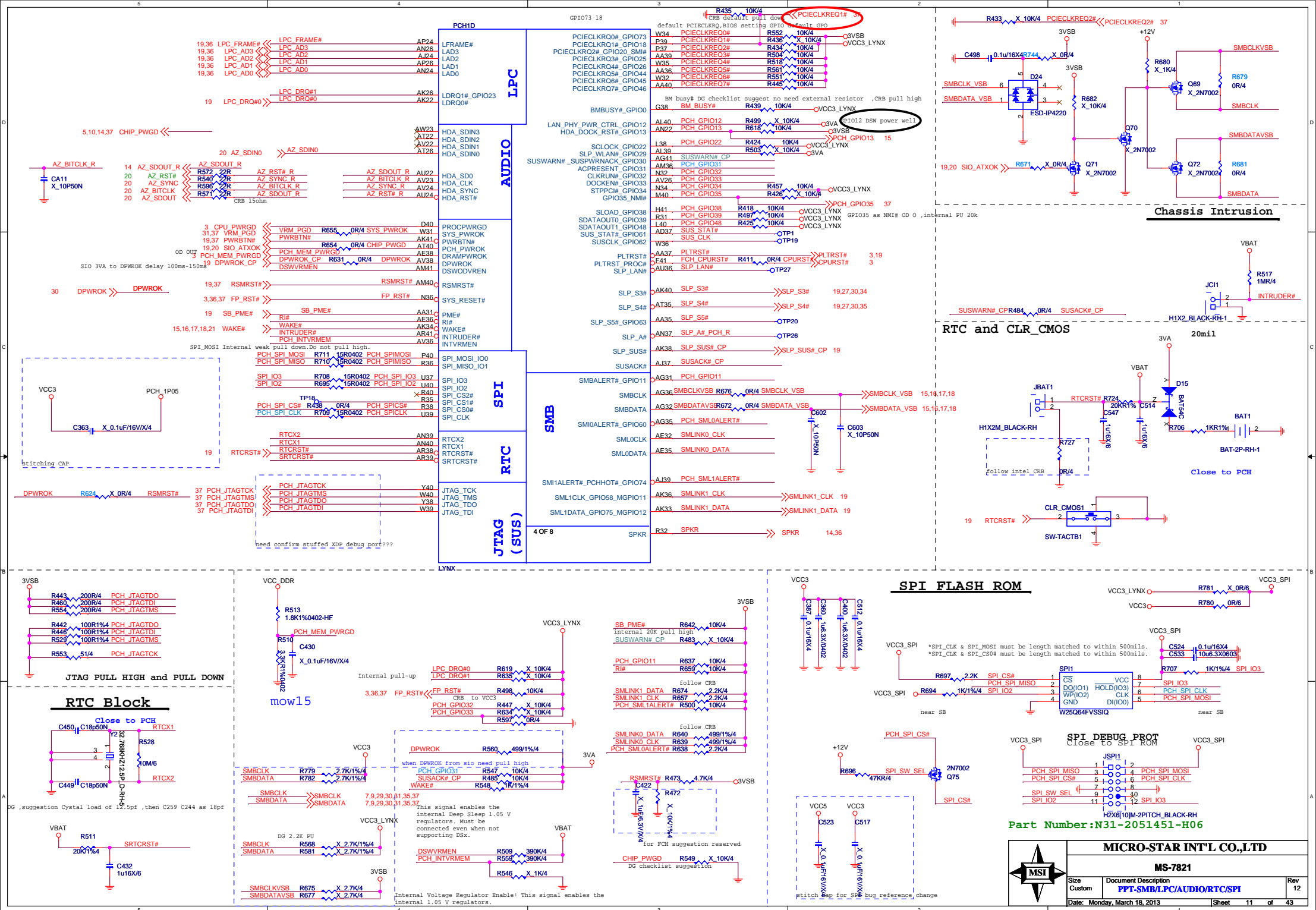


















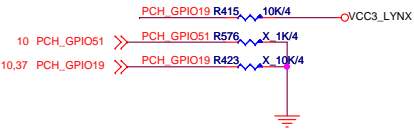




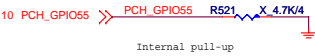
PCH Straps



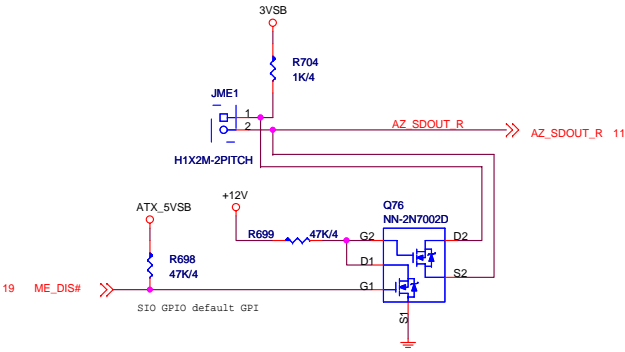
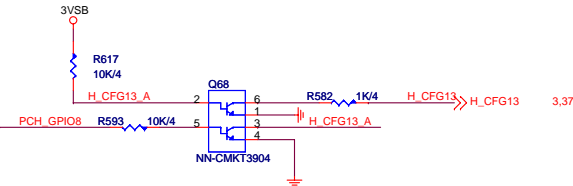
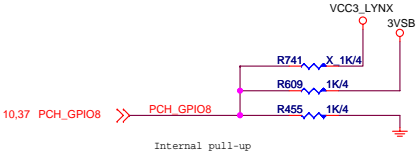
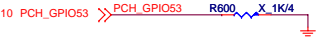
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



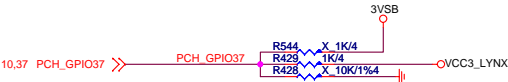
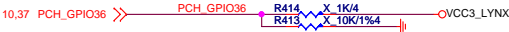
Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.



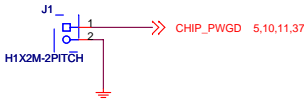
Connect to ground with 1k Ohm pull-down resistor.



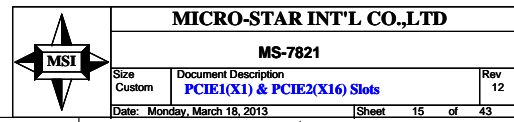
Default  
Do not pull high.  
Disable ME in Manufacturing Mode  
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



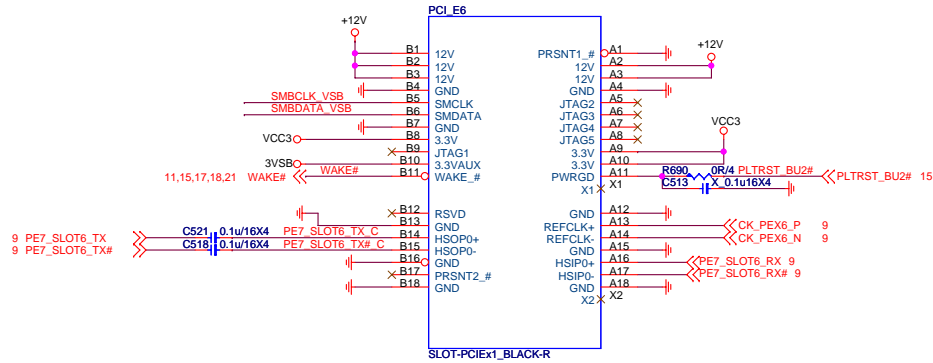
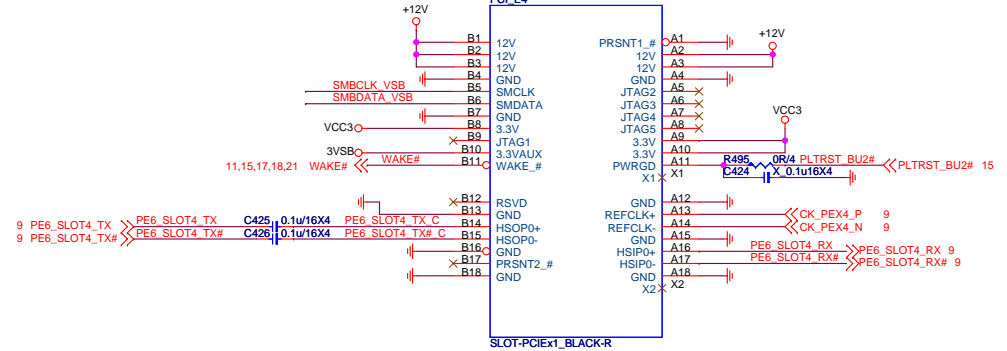
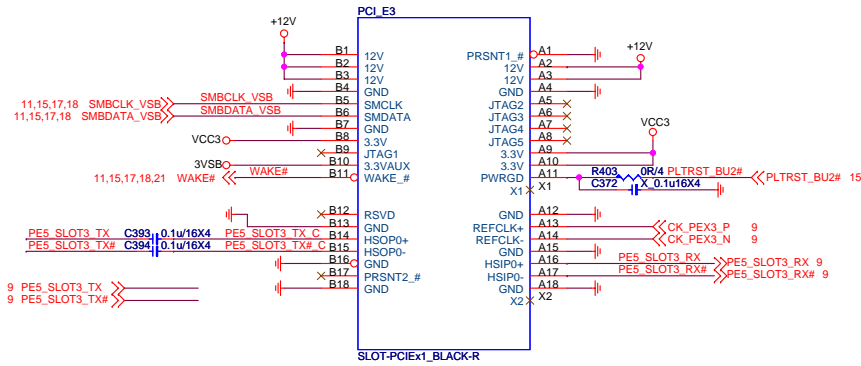
GPIO37 Enable TLS:  
Pull up with 1k Ohm to VccSus3.3.  
Default (Disable TLS):  
Leave NC. Internal pull down.











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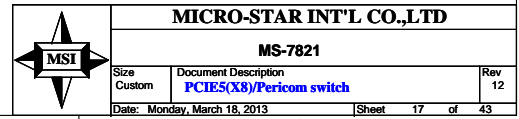
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Custom	PCIE3(X1) & PCIE4(X1) Slots	12
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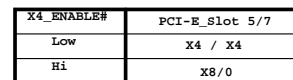
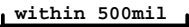
(Share with PCI\_E x16 Slots)

(Share with PCI\_E x16 Slots)





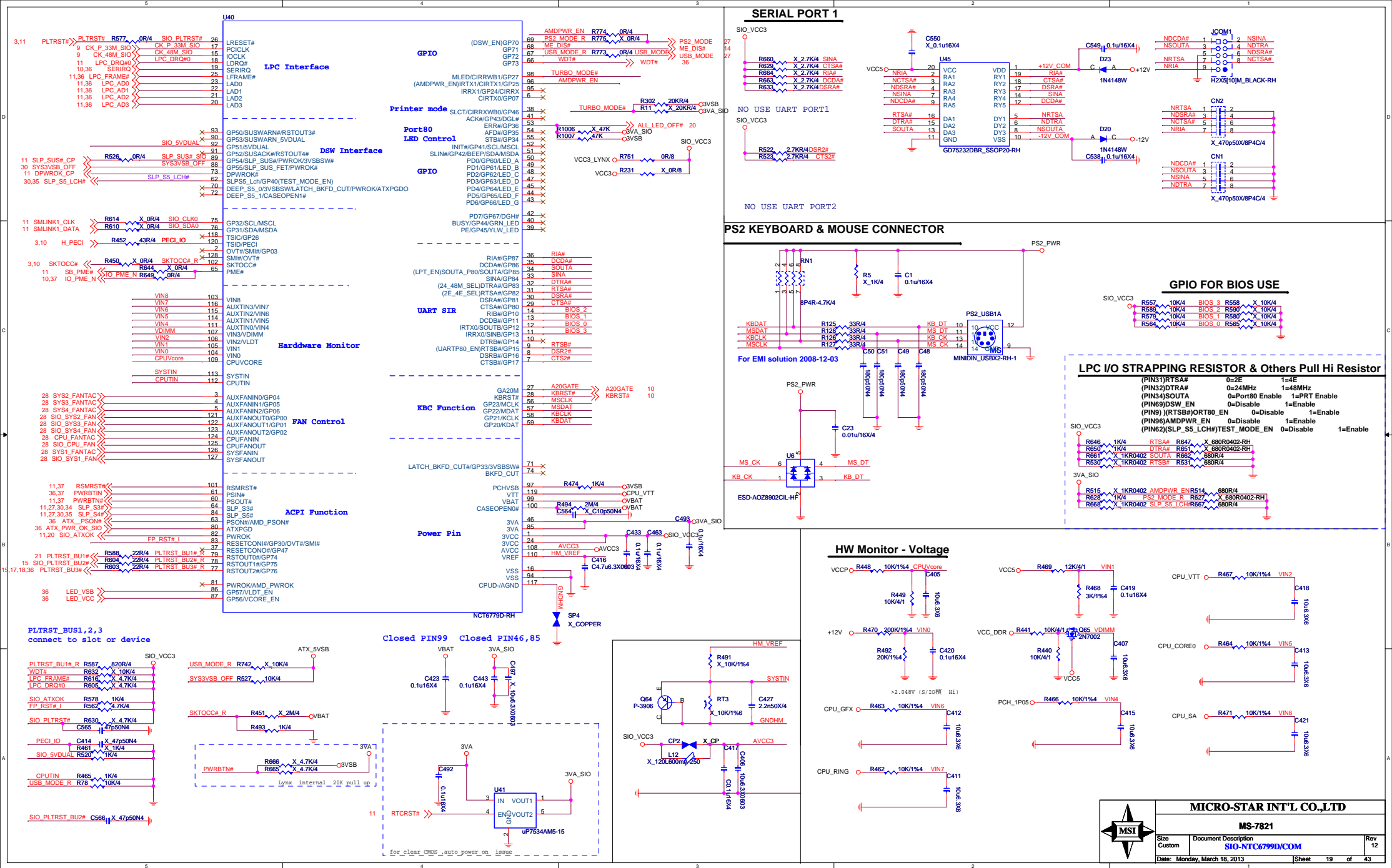
Trace width > 200 mils



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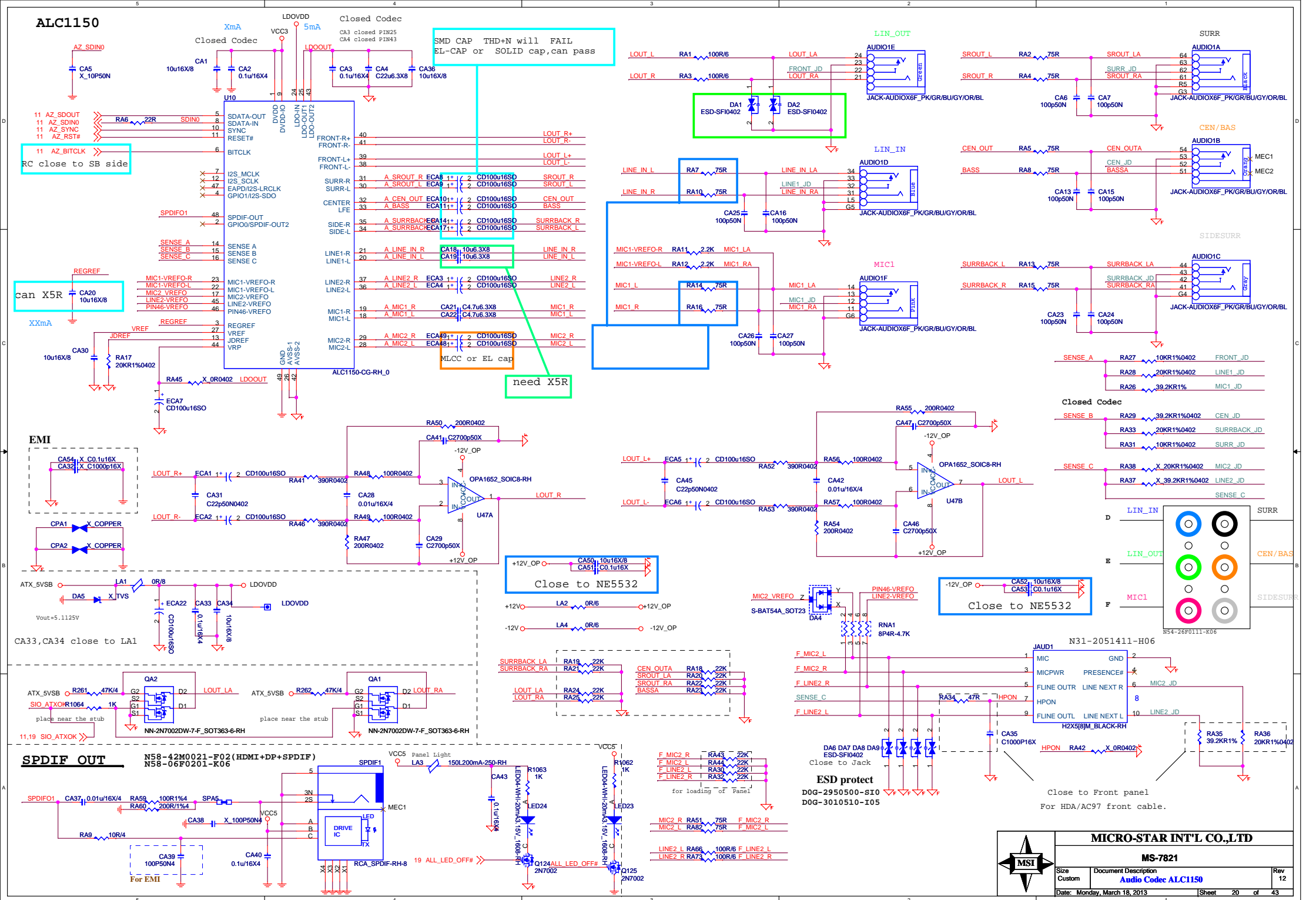
Size Custom	Document Description <b>PCIE(X4) &amp; PCIE(X1) slots</b>	Rev 12
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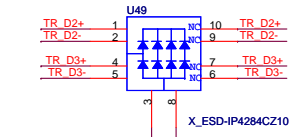
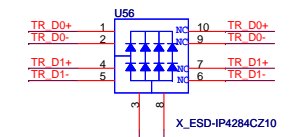
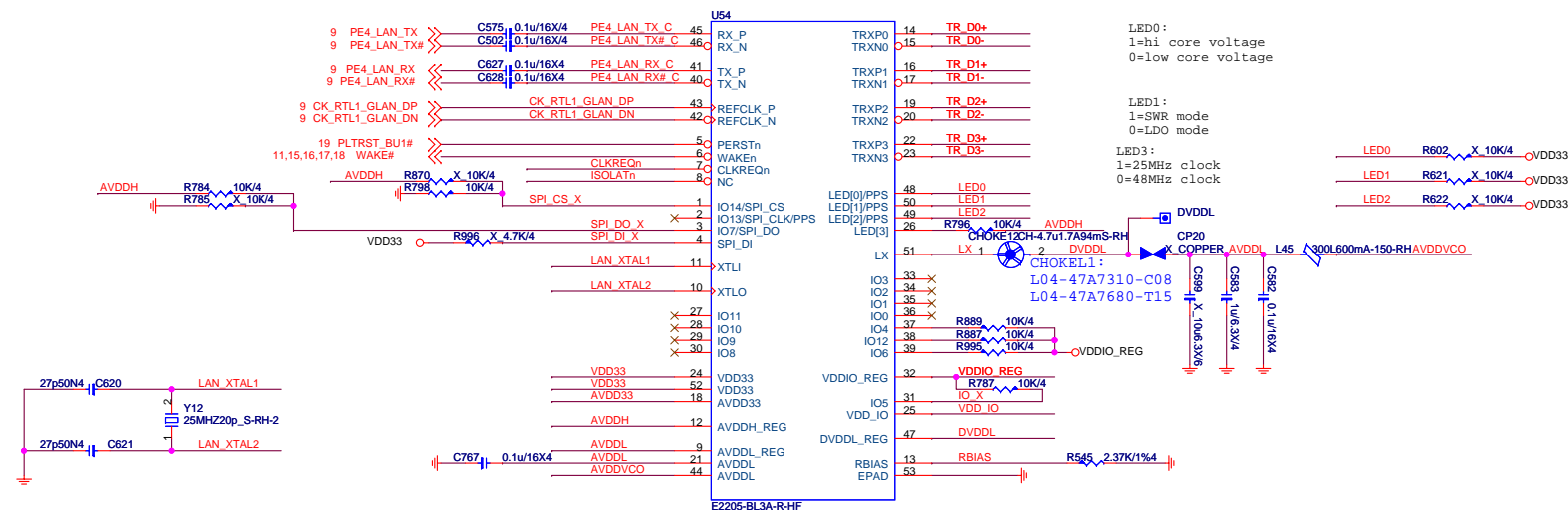




# ALC1150







D0G-05A050C-005  
D0G-05A0300-I14  
D0G-06A050C-A68

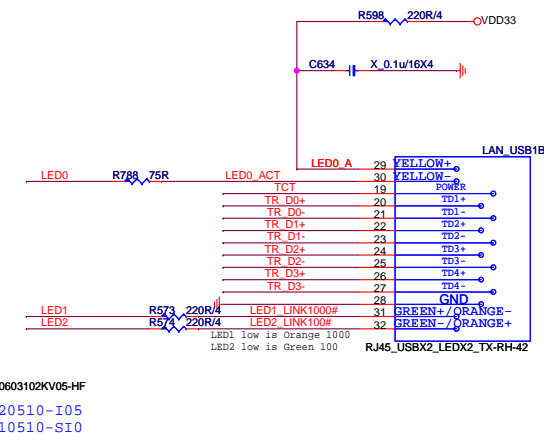
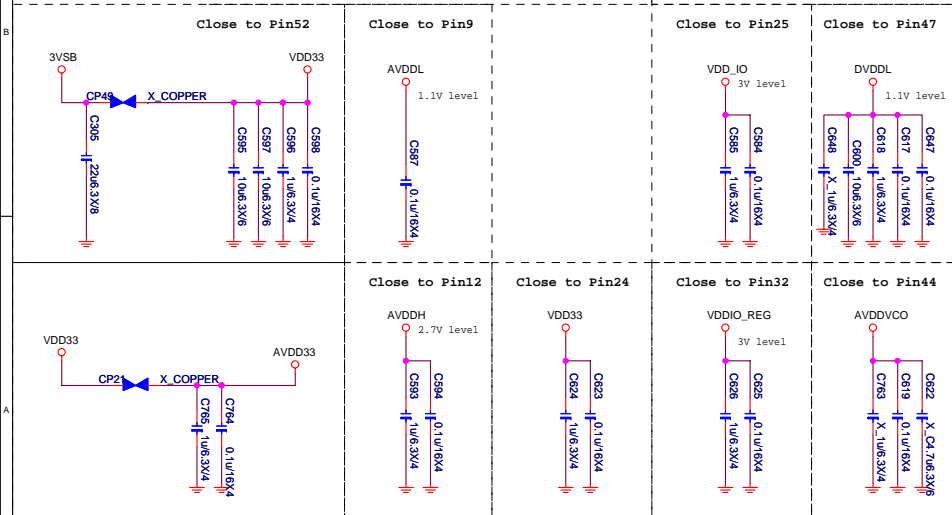
```

h0:
h. Support xD, not support SPI
Q. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
W1:
Q. Support SPI, not support xD
Q. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
W1:
h. Not support xD, not support SPI
Q. Only support PPS, PPS always at CRI013.

```

Remove pull-up R if R4 existence on motherboard  
(or SB has internal pull-up R).

```
VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDD_IO power trace should be wider than 30mils;  
VDDTIO_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.
```



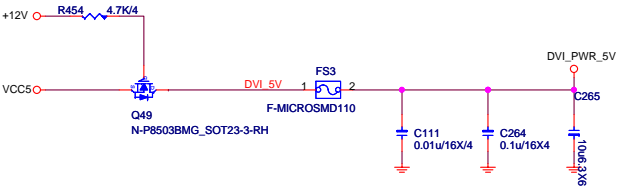
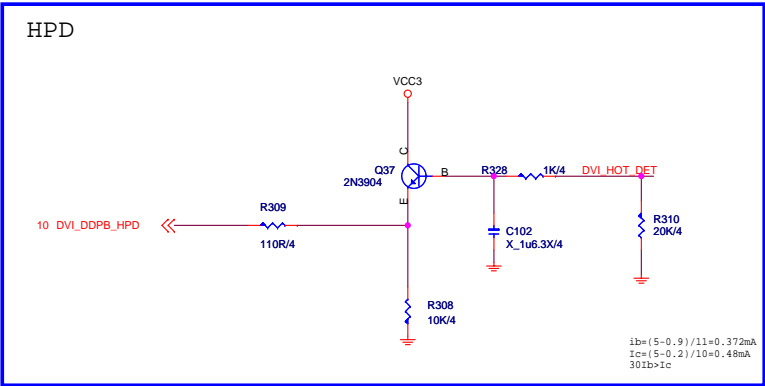
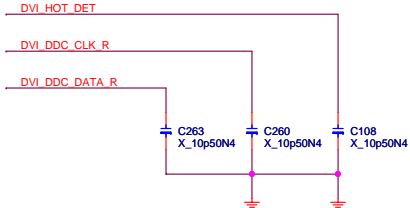
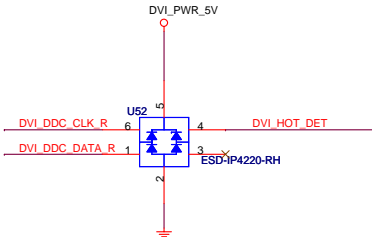
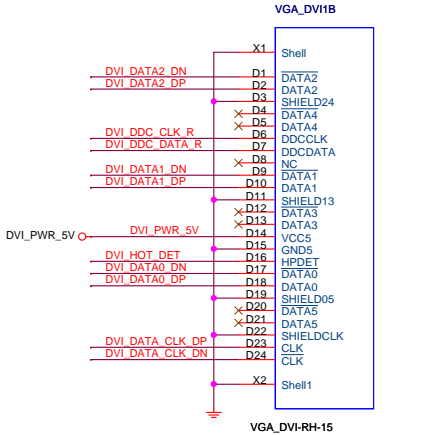
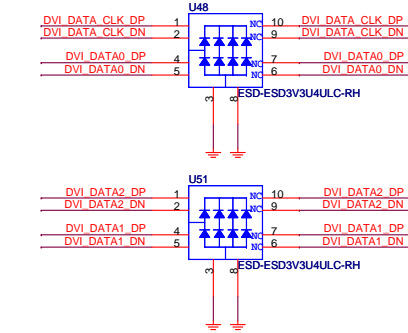
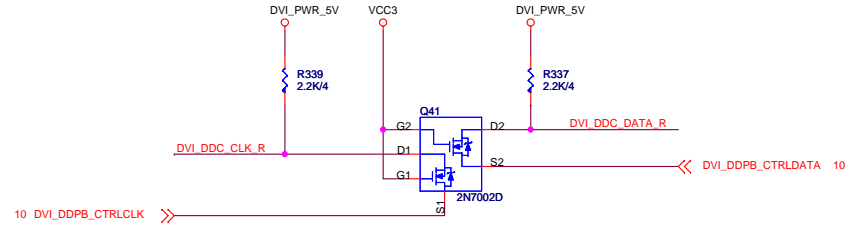
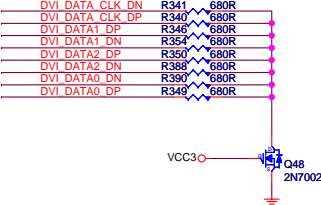
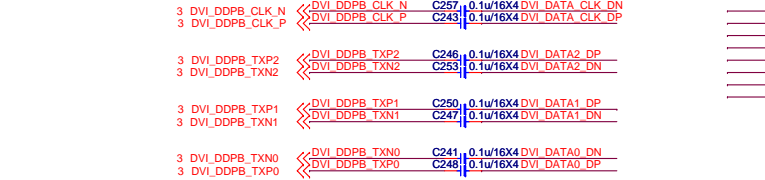
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DVI level shifter

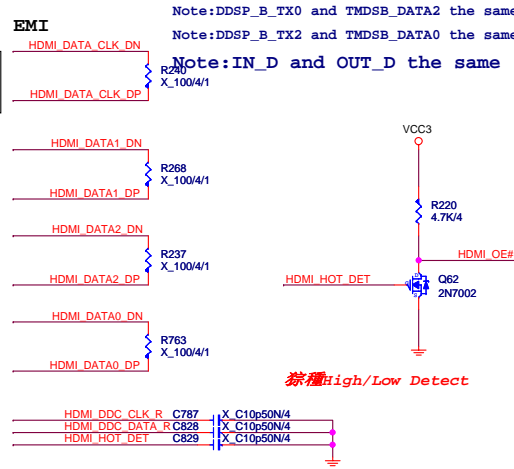
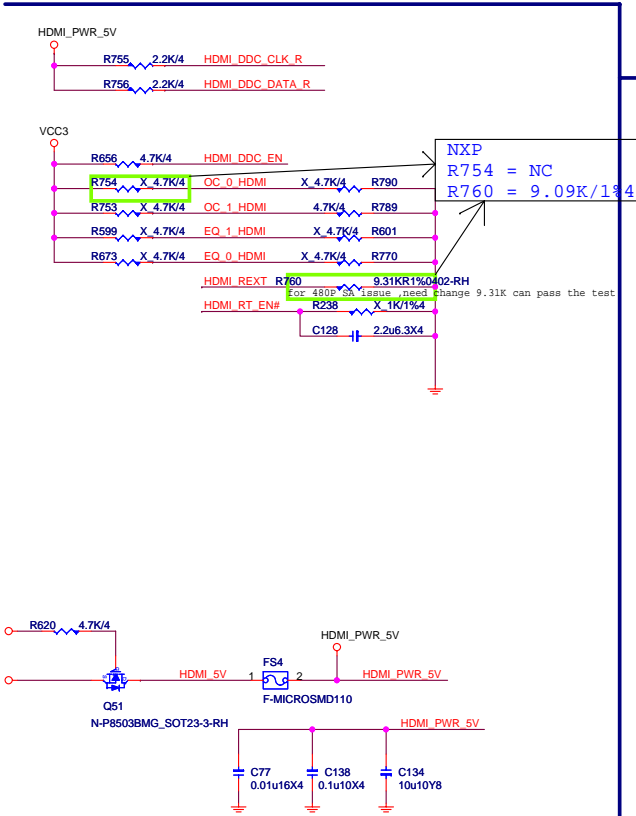
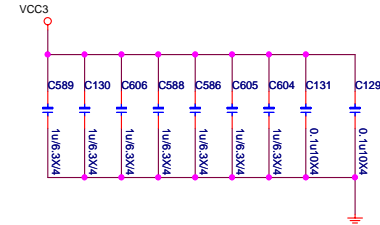
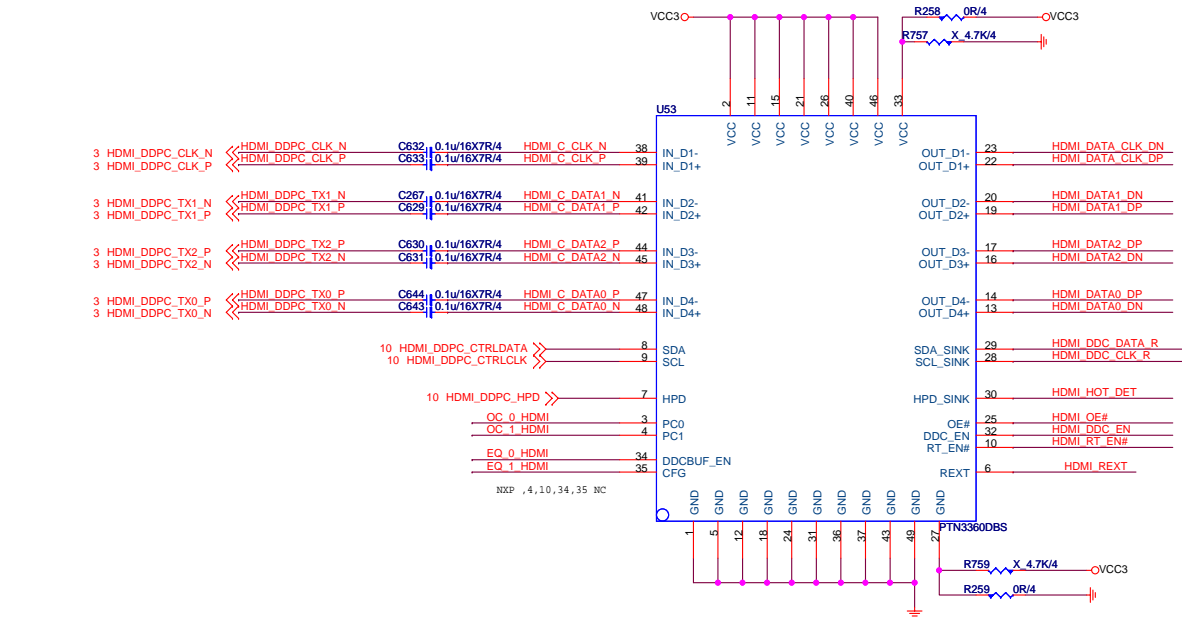


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Custom	DVI transfer	12
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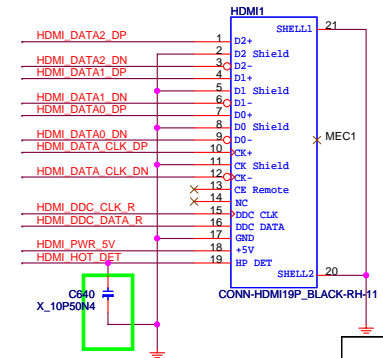


禁種High/Low Detect

Note: Reserve RN4;RN5 for EMI

	"0"	"1"	note
HDMI_DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		5V tolerant, internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PC1, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB



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**MS-7821**

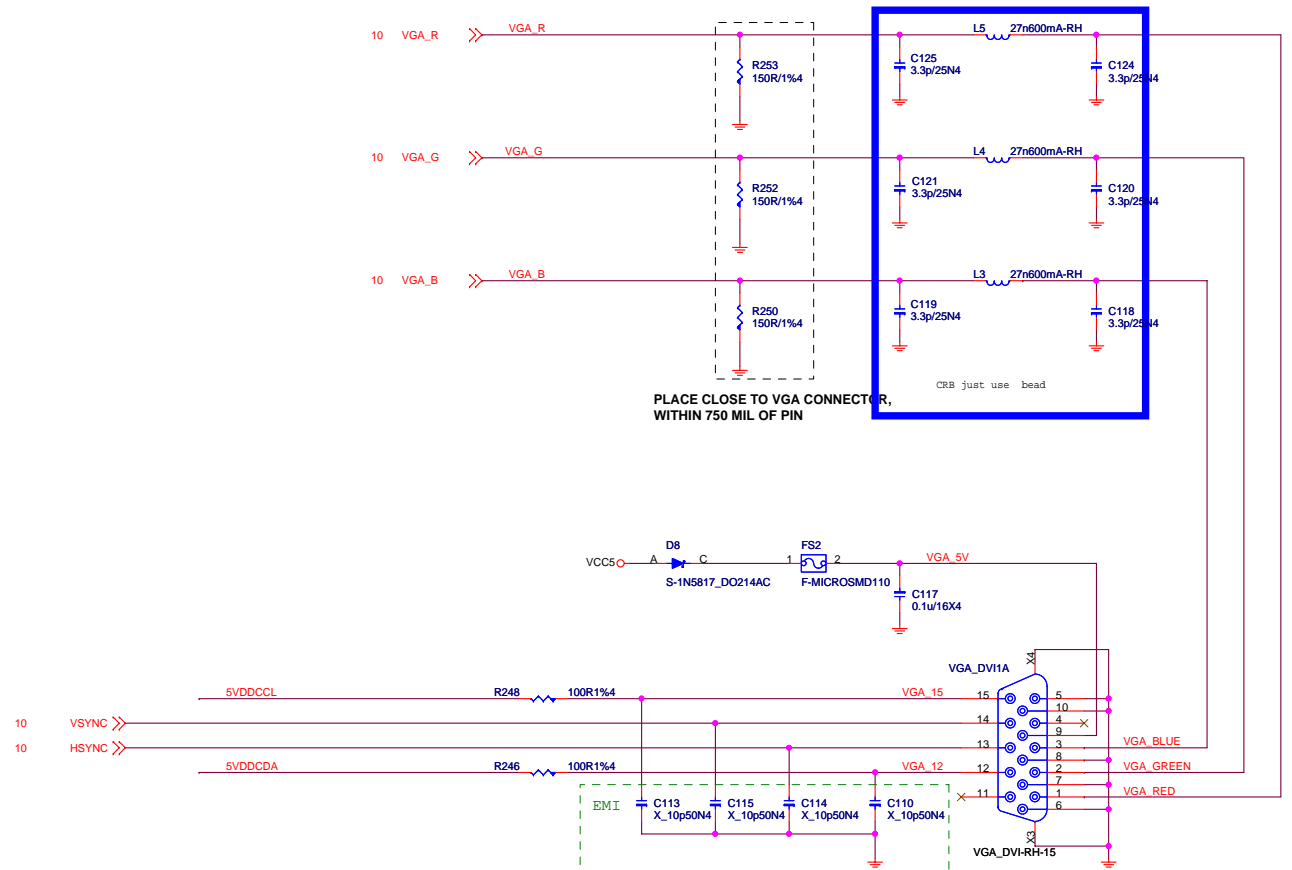
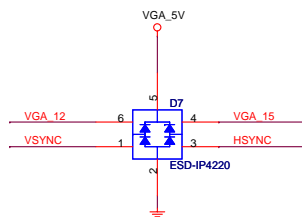
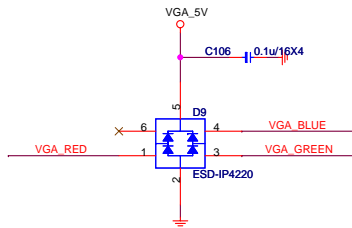
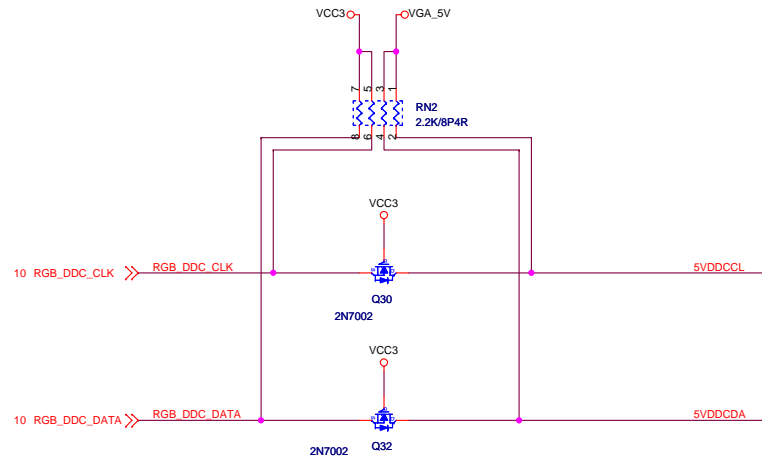
Size Custom Document Description **HDMI Connector** Rev 12

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## D-Sub

### Level shift



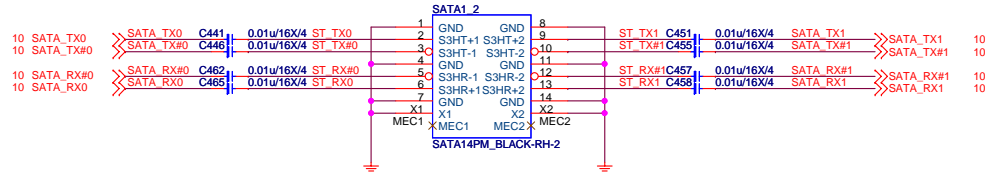
**MICRO-STAR INT'L CO.,LTD**

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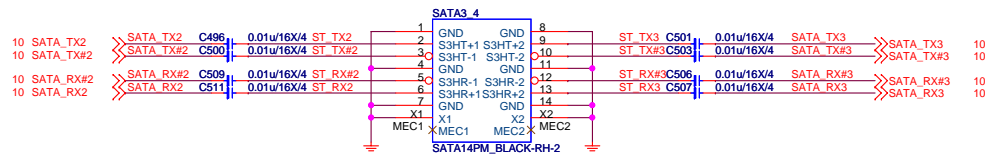
Size Custom	Document Description <b>VGA Connector</b>	Rev 12
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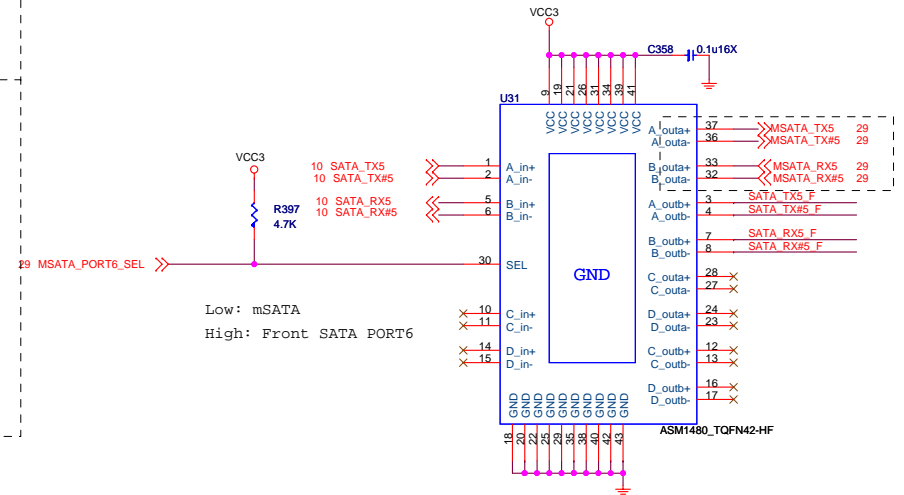
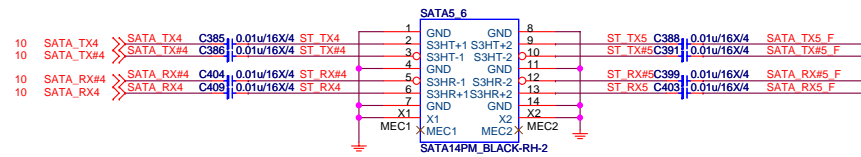
# SATA1-2



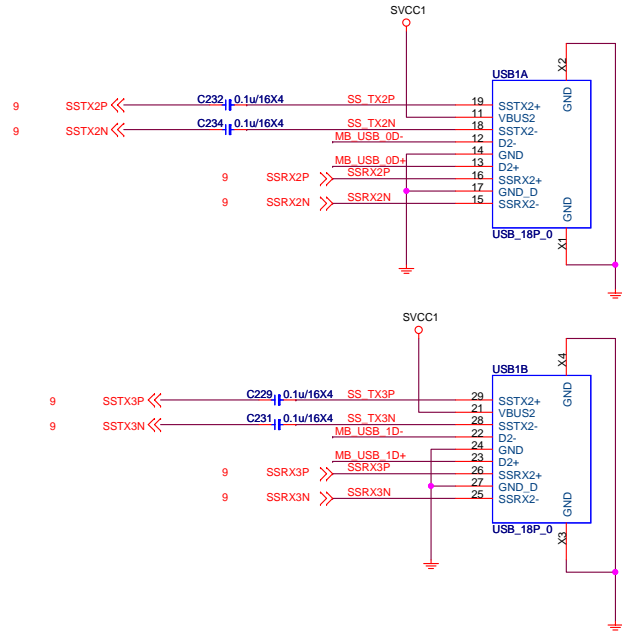
# SATA3-4



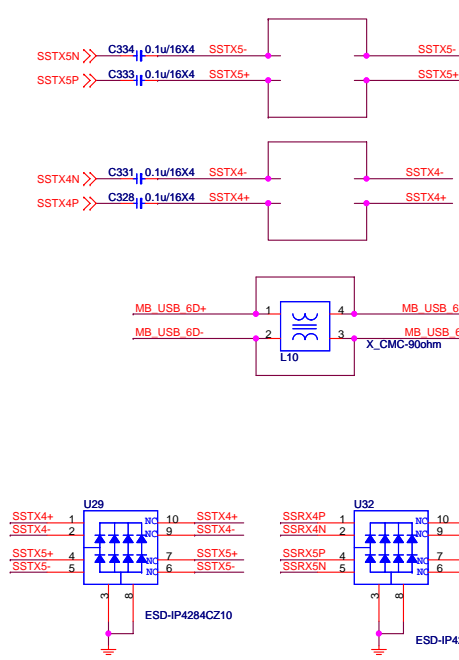
# SATA5-6



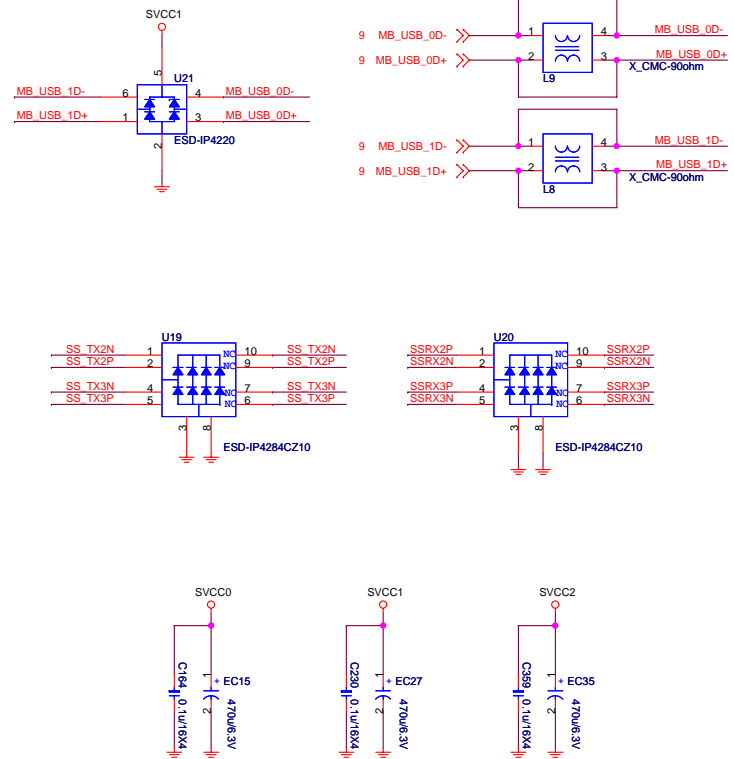




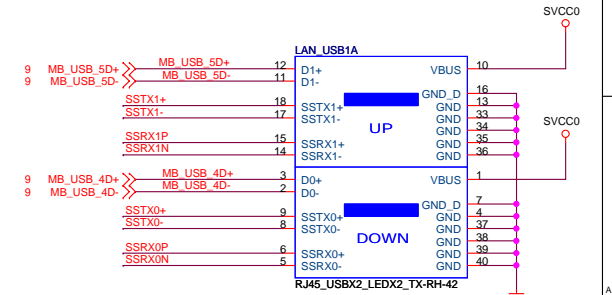
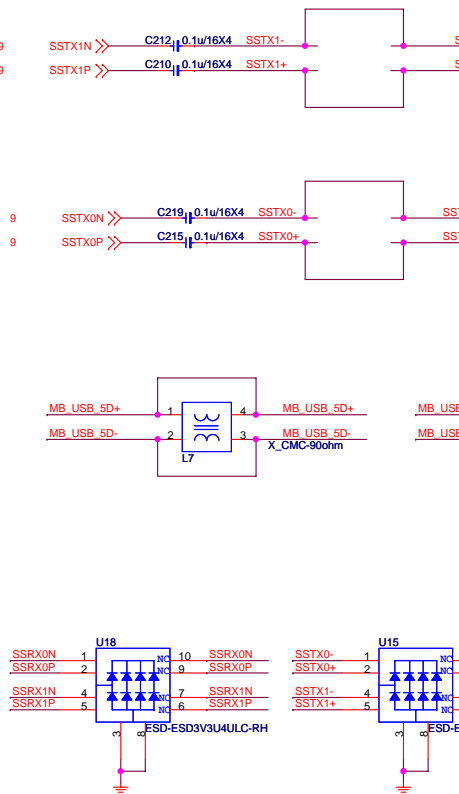
REAR USB30 PORT 2,3



FRONT USB30 PORT 0,1



REAR USB30 PORT 4,5



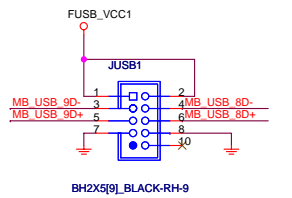
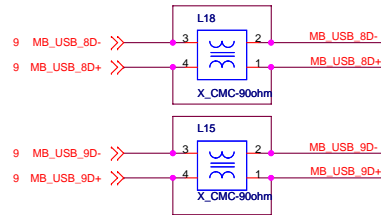
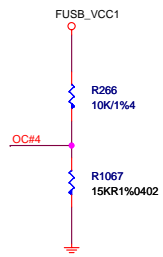
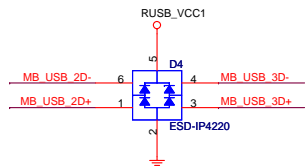
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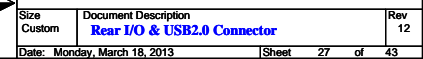
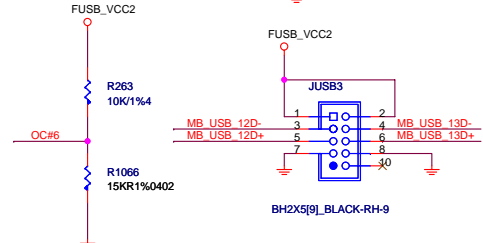
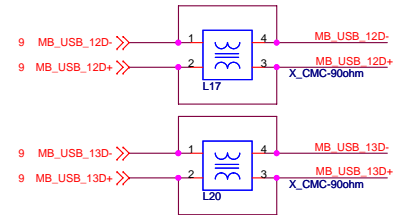
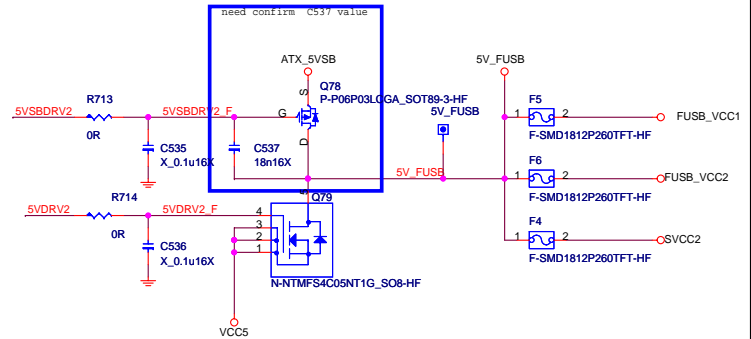
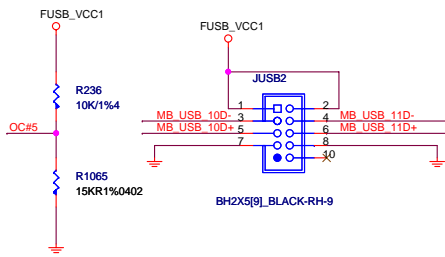
### 5VDIMM FOR DDR

7501 Mode  
H:Support S0/S3/S5  
L:Support S0/S3

Schematic diagram of the VSDRV2 pin configuration. The VSDRV2 pin is connected to a 200K/1% resistor (R689) and a 56K/1% resistor (R688) to ground. The VSDRV2\_EN pin is also connected to the same node.

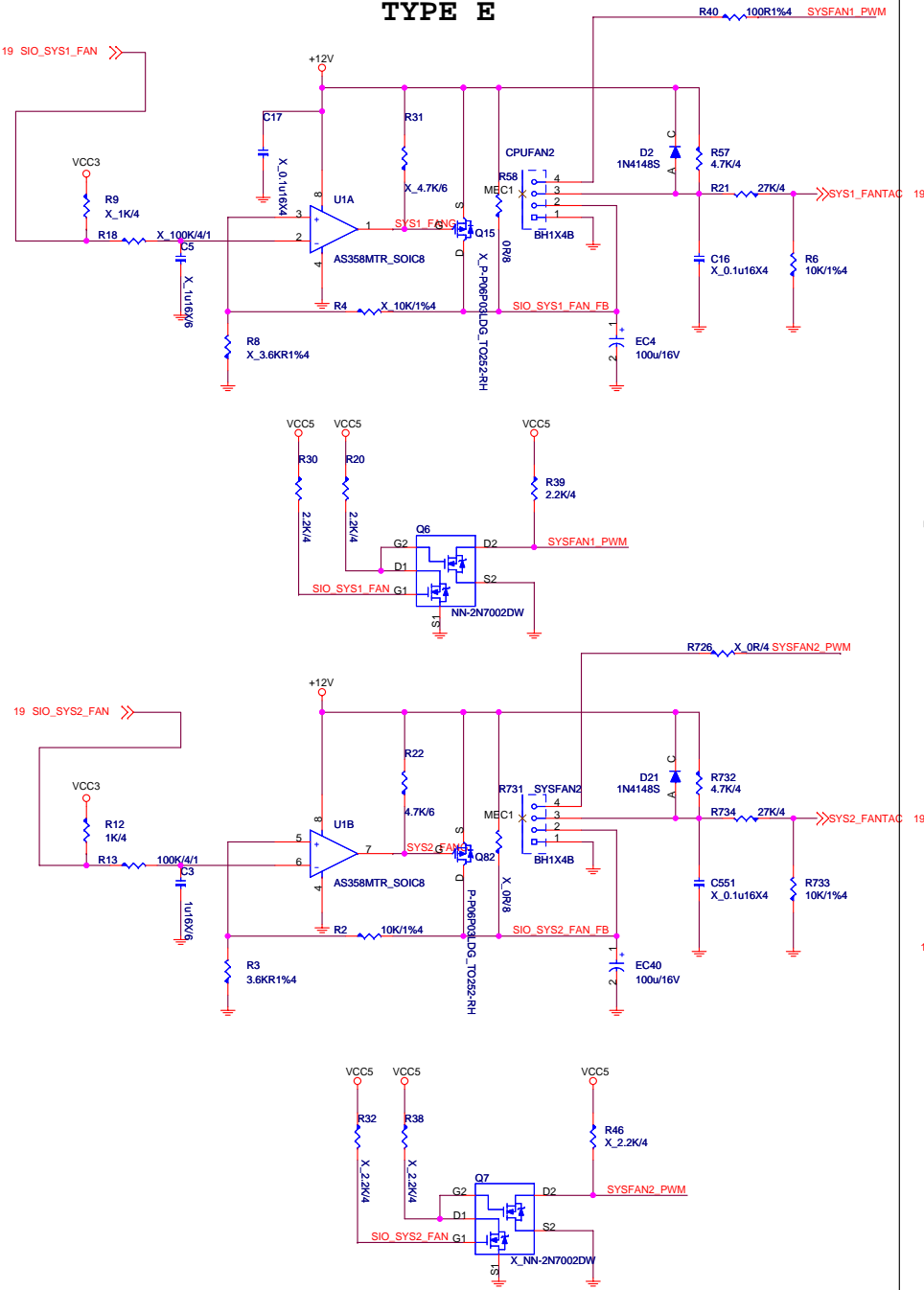


The diagram shows two identical USB interface modules, L16 and L19, connected to a common USB bus. Each module has four pins. Pins 1 and 2 are connected to the differential USB data lines (MB\_USB\_10D- and MB\_USB\_10D+ for L16, MB\_USB\_11D- and MB\_USB\_11D+ for L19). Pins 3 and 4 are connected to a common mode connection (X\_CMC-90ohm) and the USB data lines (MB\_USB\_10D+ and MB\_USB\_11D+ for L16 and L19 respectively).

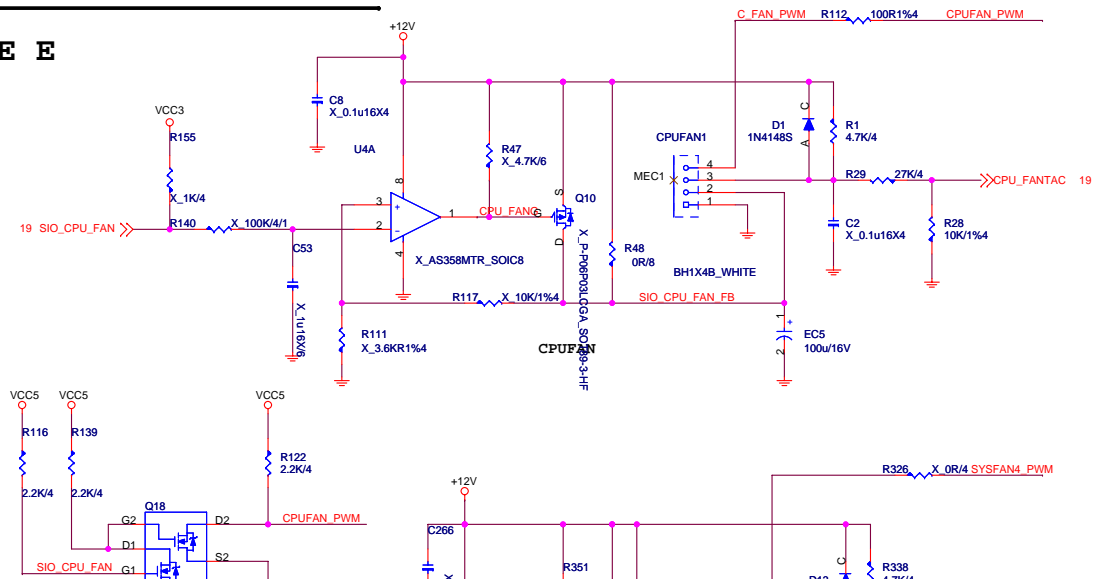




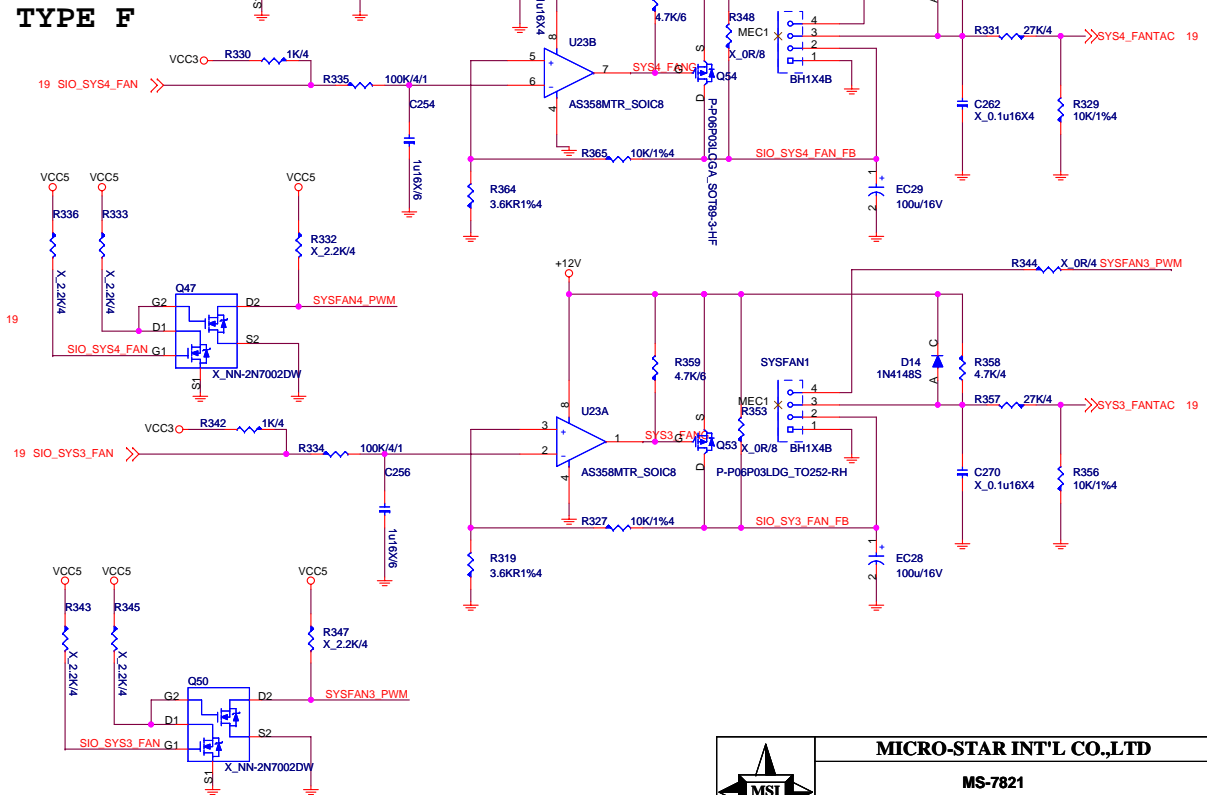
## TYPE E



## TYPE E



## TYPE F



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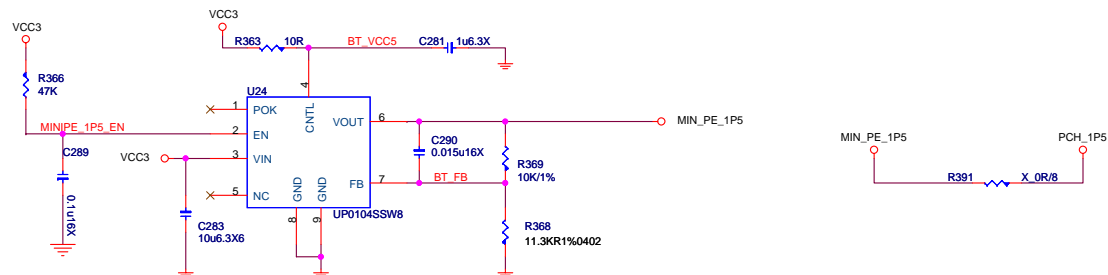
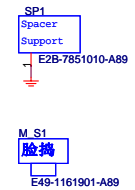
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VCC3, 1.5A

PCH\_1P5, 0.5A



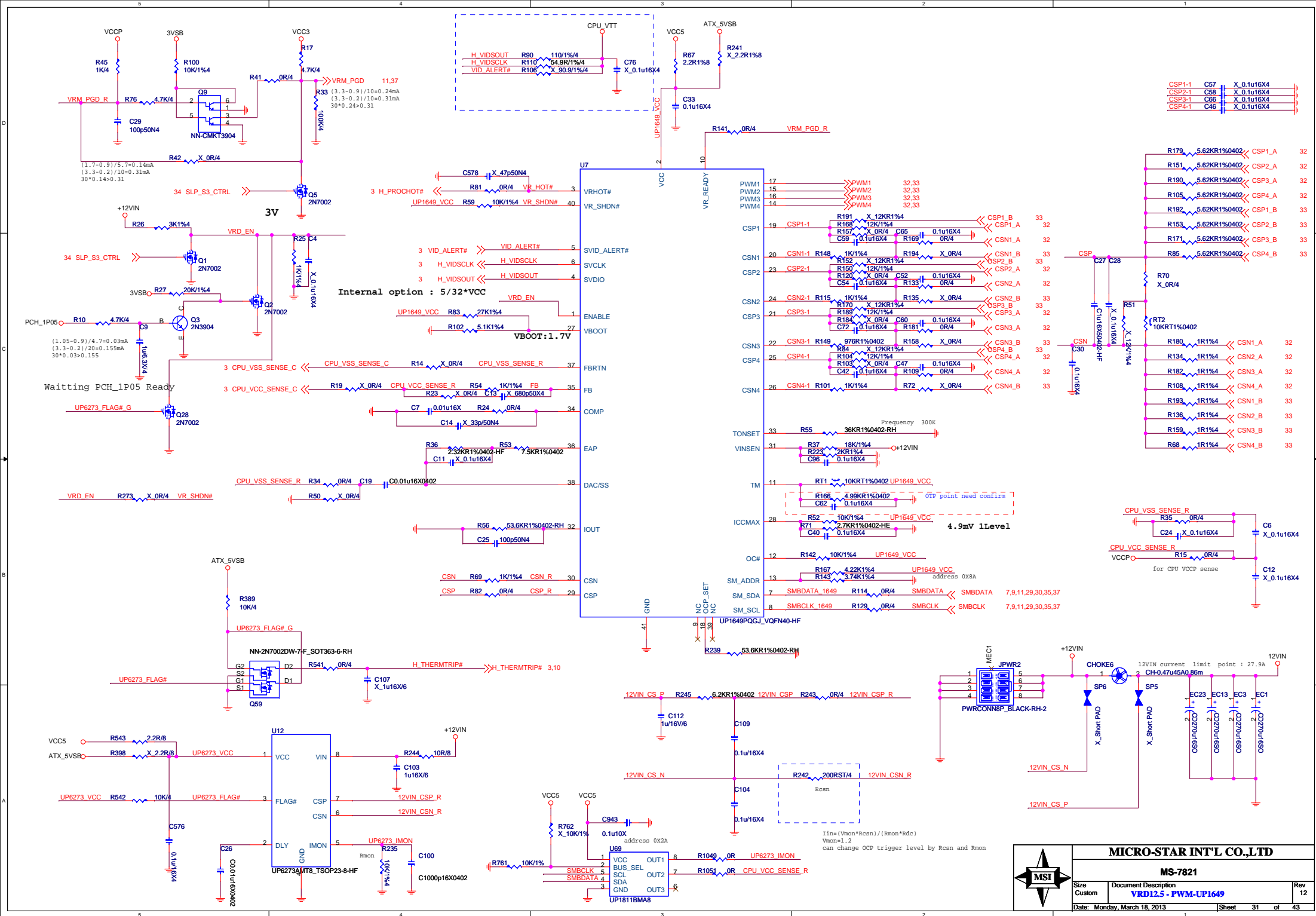
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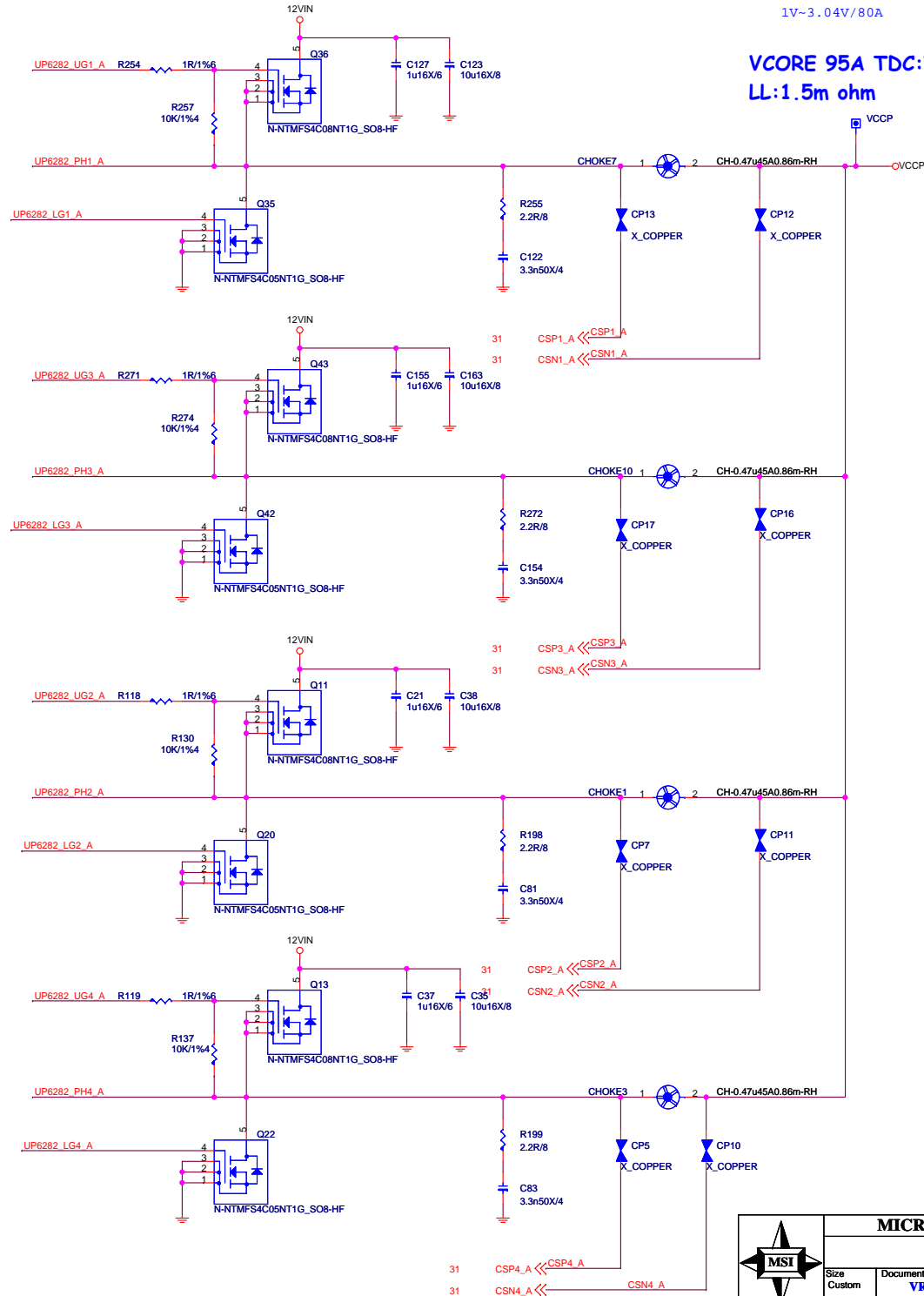
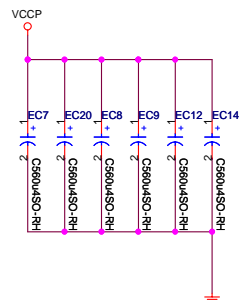
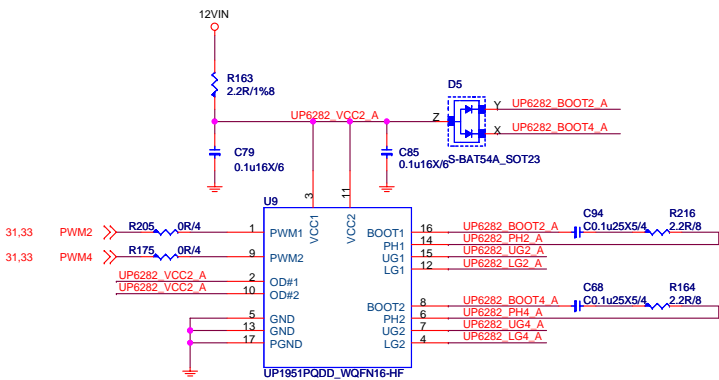
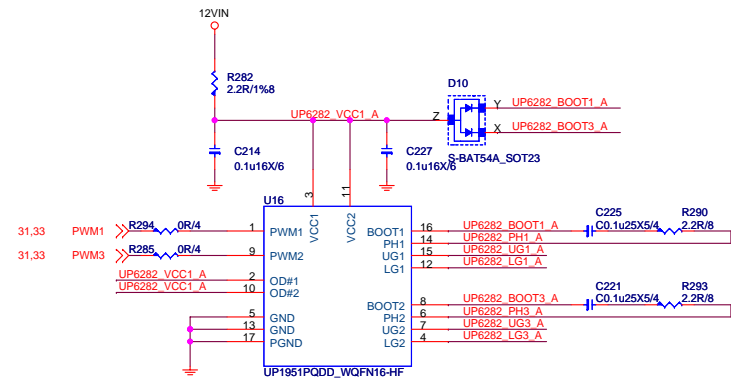




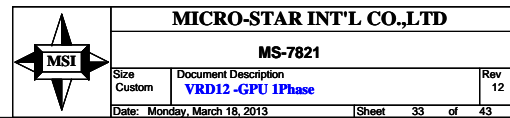
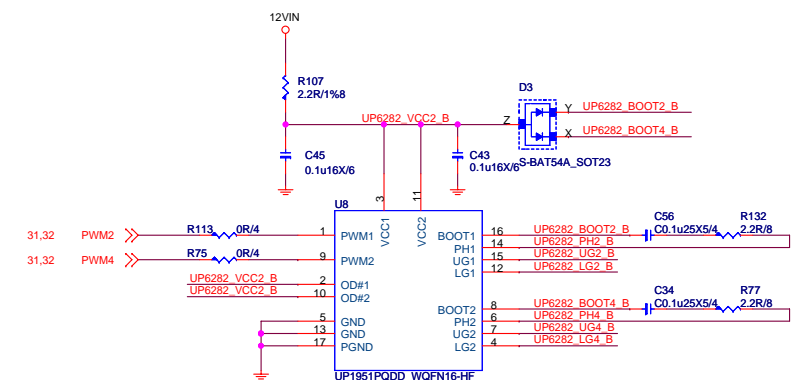












VCORE 95A TDC:70A  
LL:1.5m ohm



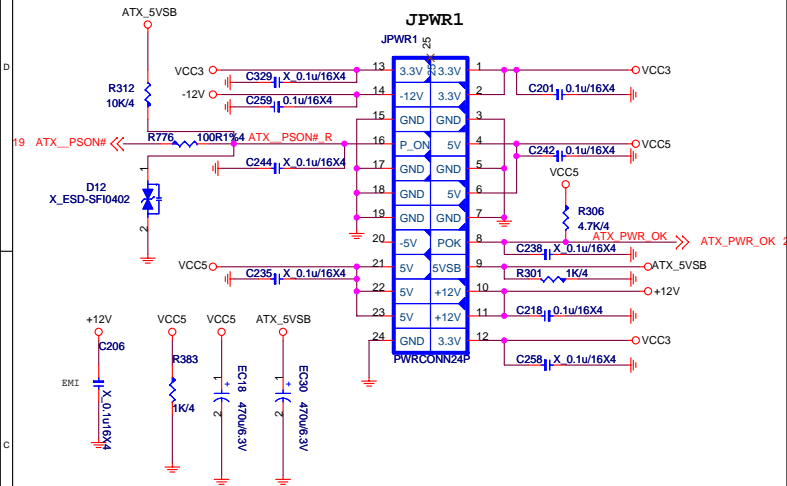




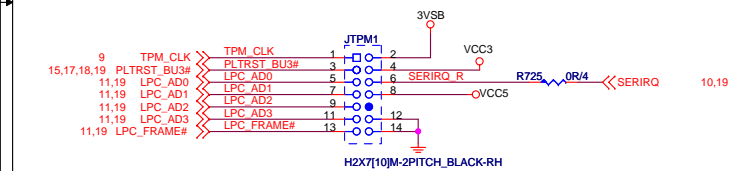




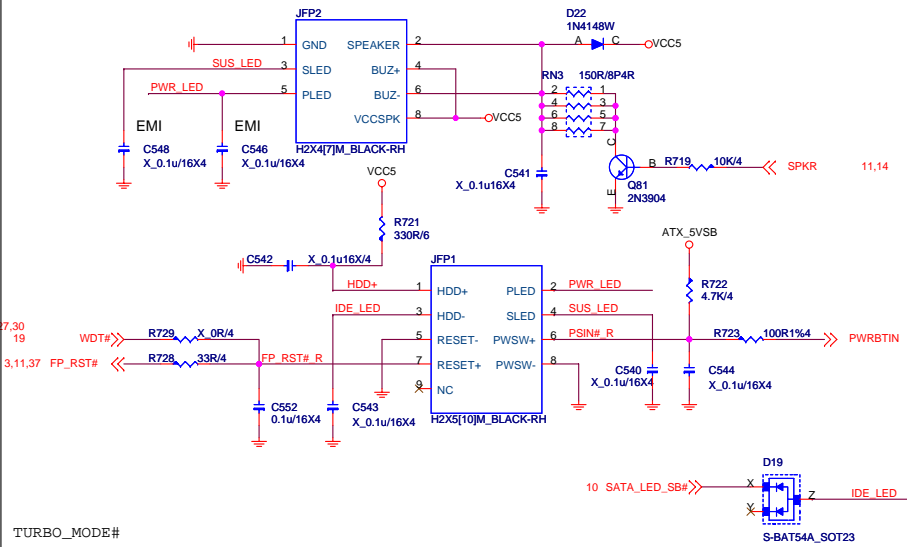
## ATX POWER CONNECTOR



**TPM**

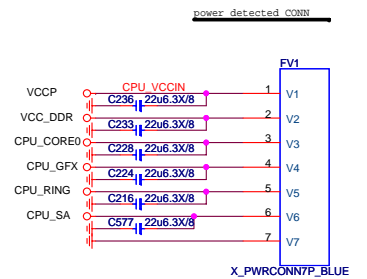
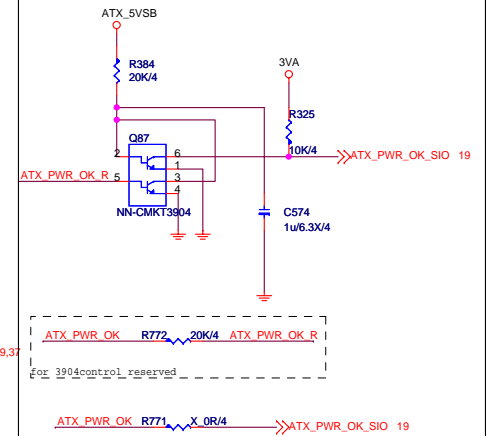
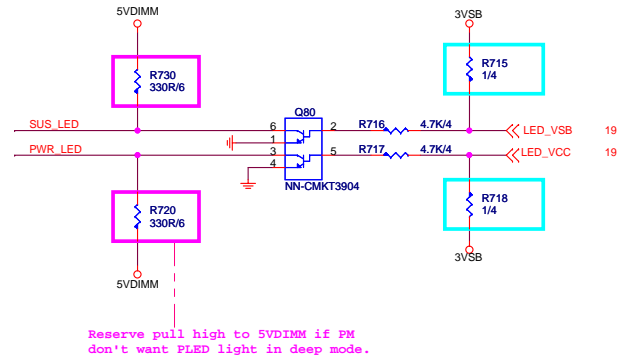


FRONT PANNEL



TURBO\_MODE#  
Default: Low,disable OC  
Push Bottom: high,Enable OC / Turn on LED

LED ( for NCT6799D)



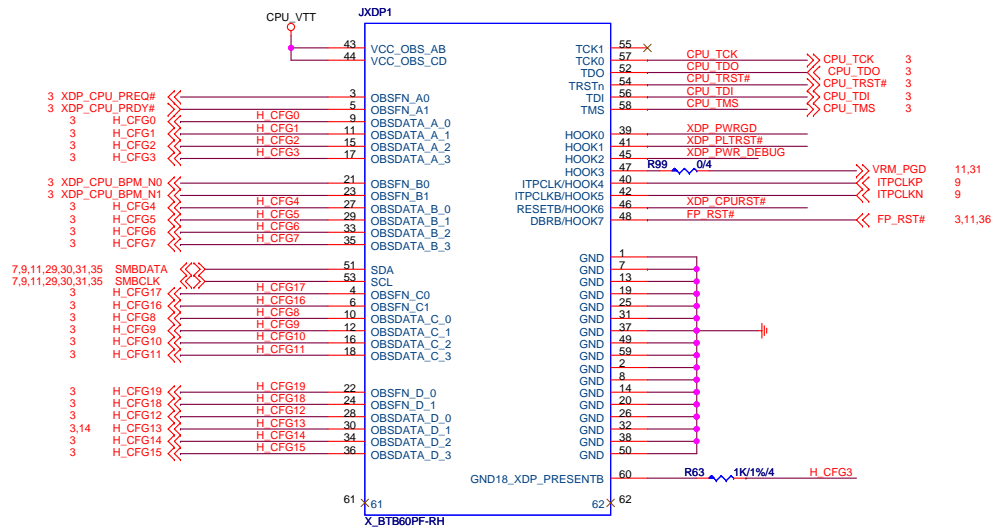
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## Reserve debug port 5020



CPU\_TDO R66 51/4 PCH\_1P05  
PLACE NEAR XDP CONNECTOR

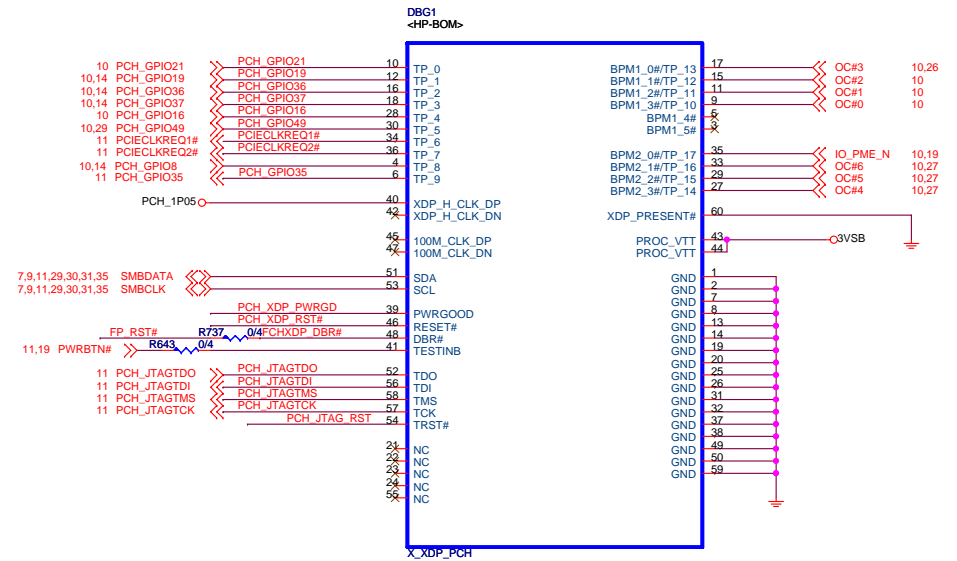
19,36 PWRBTIN >> PWRBTIN R186 0/4 XDP\_PLTRST#  
3 PWR\_DEBUG >> R211 0/4 XDP\_PWR\_DEBUG

mo15

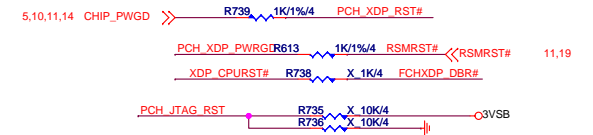
3 H\_PWRGD >> R161 1K1/4 XDP\_PWRGD

3 CPURST#\_R >> R96 1K1/4 XDP\_CPURST#

## PCH XDP



## PCH XDP PWRGD/RESET

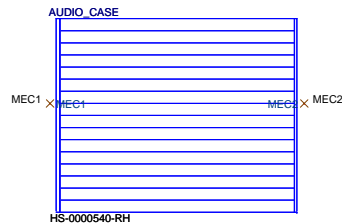
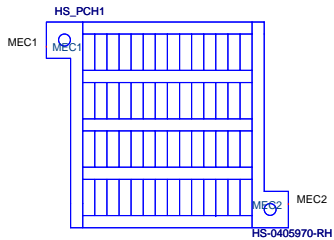
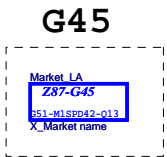
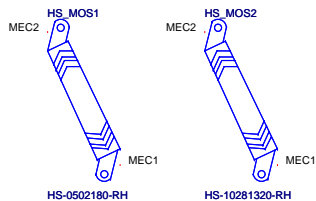


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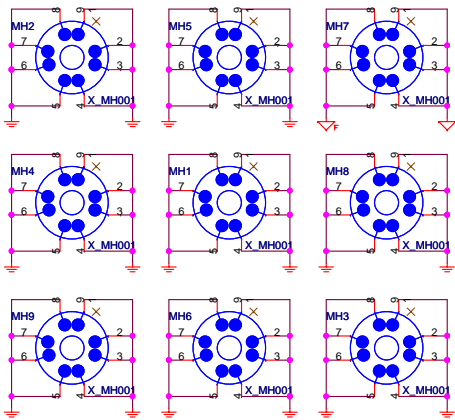
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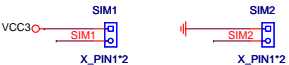




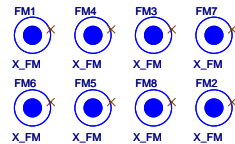
Mounting Holes



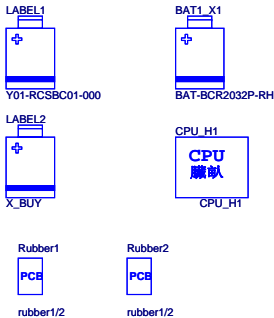
Simulation



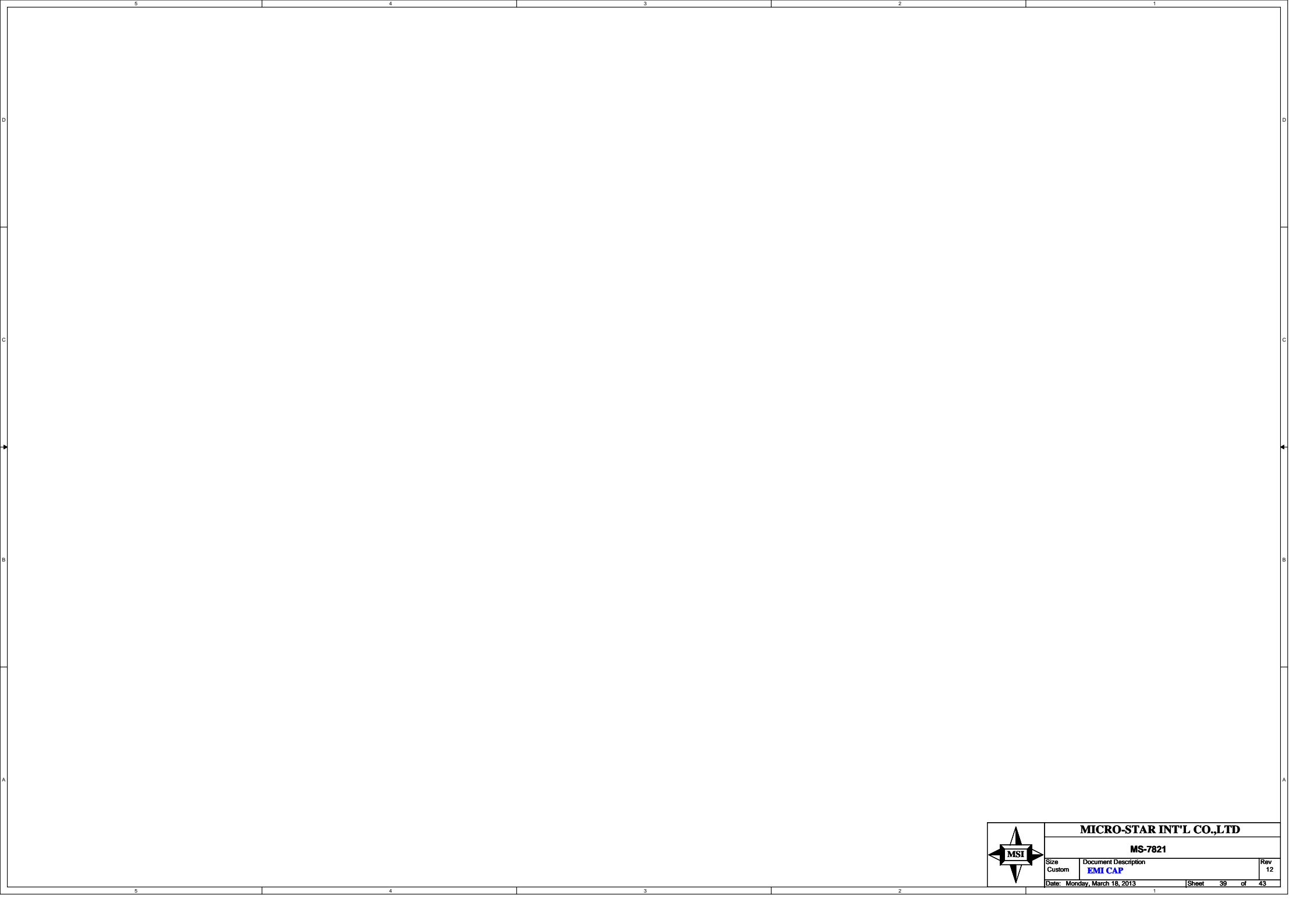
Optical Fiducial Marks-120



PCH XDP PWRGD/RESET







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